REMARKS

Claims 1-32 were pending in the Application prior to the outstanding Office Action. Claim 1 is amended to correct a typographical error. With this Amendment, claims 1-32 remain in the case.

Applicants thank the Examiner for pointing out that the Terminal Disclaimers for this application are improper. Applicants withdraw the terminal disclaimers. Any issue of obviousness-type double patenting is intended to be addressed in the related cases.

The Official Action withdraws the objection to claim 17.

The Examiner has indicated that claims 1-32 have received a second action on the merits and are subject of a final action. Presumably, this indicates that all claims are rejected for the reasons set forth in the Official Action mailed 3 January 2006.

Reconsideration is respectfully requested. In particular, Applicant disagrees with the Examiner's finding that Allegrucci teaches an integrated circuit that includes memory "storing instructions for a mission function for the integrated circuit, storing instructions for a configuration load function used to receive configuration data via said input port, and storing instructions for a configuration function used to transfer the configuration data to the programmable configuration points within the configurable logic array; ..." as stated in independent claim 1.

The Examiner provides four citations to Allegrucci in support of the rejection. Each of the citations is considered. The first three citations fall within the text at column 2, lines 24-54, reproduced here:

A high-performance internal system bus **115**, which may be a Configurable System Interconnect (CSI) bus, for example, interconnects the microcontroller **105**, its peripherals **130**, and the CSL matrix **120** at a speed of 66 MHz, for example. In one embodiment, the bus **115** provides 32 bits of read data, 32 bits of write data, and a 32-bit address. Multiple masters arbitrate for bus access. Potential bus masters include the microcontroller **105**, the JTAG interface **135**, the read and write channels of each DMA channel, and the memory interface unit **140** (MSSIU) in some modes of operation. Functions implemented in the CSL matrix **120** can use a DMA channel as a "proxy" master, re-using the control logic already contained in the DMA channels to become a master on the CSI bus **115**. The CSI, as well as the local CPU bus **145**, may follow the little endian format.

A static memory interface unit (part of the memory sub-system MSSIU **140**) connects the configurable processor **120** to external static memories of the type FLASH or SRAM. The MSSIU **140** can connect to an external FLASH memory device that holds an initialization program plus the user's code. The MSSIU interface is reusable for connections to other external components. The external read, write, control, and chip-select signals are programmable providing flexible set-up, strobe, and hold timing. A direct connection from the CPU **105** to the MSSIU **140** (bypass mode) is provided to remove any additional latency incurred going through the CSI **120**. For low frequency applications, the microprocessor **105** can fetch its instructions from the external FLASH directly. Assuming a FLASH with a one cycle access time, non-sequential accesses from the microprocessor incur one wait state, while sequential accesses incur no wait states.

Support for external dynamic memories provides the user

First, the Examiner takes the position that the entire section just reproduced "covers the configuration function." Applicant points out that the claim requires instructions stored in memory on the integrated circuit "for a configuration function." The first paragraph of the cited passage describes a bus system on the Allegrucci system that could be used for configuration, but does not mention where the instructions for the configuration function are stored.

The second paragraph of the cited passage describes a memory interface unit for connection to external memory that "holds an initialization program plus the user's code." The Examiner takes the position by implication that the claim limitation describing memory on the integrated circuit storing instructions for a configuration function reads on Allegrucci's "initialization program plus the user's code" stored in external memory. This is mistaken because first, Allegrucci places the "initialization program plus the user's code" in external

memory. This is mistaken second, because there is no basis for concluding that the "initialization program plus user's code" includes instructions for a configuration function.

In addition to the fact that the claim requires memory on the integrated circuit, and Allegrucci relies on external memory, the Examiner apparently is taking the further mistaken position that a configuration function is inherent in the initialization program. However, in order for the instructions for configuration function to be inherent in the initialization program, such instructions must necessarily be present in the initialization program. Applicant suggests that Allegrucci in fact suggests that the instructions for the configuration function are not part of the initialization program.

In Allegrucci, the configurable system logic 120 is connected directly to the "Configuration Unit" in the memory interface unit 140. Allegrucci does not describe the configuration function for the configurable system logic 120. Allegrucci states that an initialization program is loaded from external memory, but does not state what is being initialized by the program. The Examiner apparently interprets this "initialization program" as the configuration instructions of claim 1. However, the claim requires that the configuration instructions be "fetched and executed by the processor". In Allegrucci, the configuration function is apparently independent of instructions executed by the microprocessor 104

In fact, Allegrucci suggests that the configuration function does not include instructions executed by the microprocessor 104, by including a distinct element in the block diagram labeled "Configuration Unit" and emphasizing that the Configuration Unit "connects the configurable processor (sic - system logic) 120 to external static memories..." Col.2, lines 38-40. This suggests in fact that instructions for configuration are not part of the externally stored initialization program, but rather the configuration function is embedded in the "Configuration Unit." Thus, Allegrucci suggests that the instructions for the configuration function are not part of an initialization program executed by the processor, and are instead embodied in some unspecified manner by the "Configuration Unit" -- the structure of which is not described.

Thus, as to the "instructions for a configuration function" recited in claim 1, the Examiner's position is mistaken because the claim requires such instructions to be stored in on-chip memory, and because there is no evidence that the "initialization program" of Allegrucci includes instructions for a configuration function.

The Examiner takes the position that the claimed "instructions for a configuration load program" reads on Allegrucci, citing column 3, lines 30-35. This passage is reproduced as follows:

> Power management control provides selectable power-down options over internal functions. Furthermore, each PIO provides pin-by-pin power-down settings. An internal initialization boot ROM controls the start of initialization after power-on or after the reset pin is released. The primary purpose of the initialization boot ROM is to find the user's initialization data and code stored in the secondary boot code, usually held in external nonvolatile memory. Initialization programs can be written to external flash via JTAG through the MSSIU interface.

This passage refers to an initialization boot ROM, used to store instructions that control the start of initialization. The passage does not mention loading configuration data for a configurable logic array. Rather, it describes finding a user's initialization code. The functions executed by the initialization code are not related to configuration of the configurable logic in Allegrucci as discussed in detail above, either literally or inherently.

The configuration load function of the claims is "used to receive configuration data via said input port." The configuration data is then transferred according to the claim by the instructions for a configuration function to programmable configuration points in the configurable logic array. The initialization boot ROM stores instructions for finding initialization code. There is no basis in this record for equating the initialization code of Allegrucci with such configuration data. The functions executed by the initialization code are not related to configuration of the configurable logic in Allegrucci. As discussed in detail above, the configurable system logic 120 of Allegrucci is apparently configured by the "Configuration Unit" without involvement of the microprocessor.

Thus, as to the "instructions for a configuration load function" recited in claim 1, the Examiner's position is mistaken because the initialization boot ROM stores code for finding initialization program executed by the processor in Allegrucci, not for finding configuration data as required in the claim.

Each of the other independent and dependent claims in the present application distinguish over the references for at least the same reasons, as set forth in detail in the Amendment filed 24 April 2006, which is incorporated by reference.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested. If the Examiner believes a telephone conference would aid the prosecution of this case in any way, please call the undersigned at (650) 712-0340.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1520-1).

Respectfully submitted,

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